

Título do trabalho

Autor1 A. B. Fulano, Autor2 A. B. Ciclano and Autor3 A. B. Beltrano

LSERF / FEEC / University of Campinas (Unicamp)

Barão Geraldo/University City - Campinas-SP, Brazil

(fulano, ciclano, beltrano)@dsif.fee.unicamp.br



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Laboratório de Soluções em Eletrônica e RF

Introduction

This work describes the structure and operating concepts about LC Resonance Voltage-Controlled Oscillators (LC-VCO) for application in Phase-Locked Loop (PLL)-based Frequency Synthesizers, considering the equivalent electrical model, resonance frequency, active load structures and varactor operation. For illustration of the referred concepts, a case study is presented in the final section of the work for performance parameters characterization (output frequency, frequency tuning characteristic and phase noise) considering a schematic level implementation with power supply VDD = 1.8 V at Cadence development environment by applying CMOS technology.

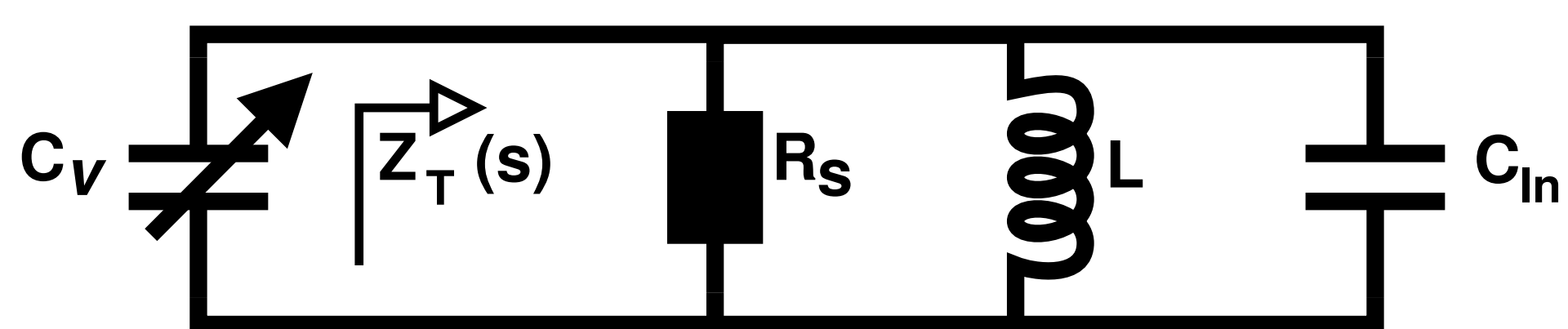
Section 1

An oscillator implemented with CMOS technology can be designed in different ways. Can make use of harmonic circuits that generate almost sinusoidal outputs or non-linear circuits that provide non-sinusoidal outputs (square, triangular, ramp or pulse).

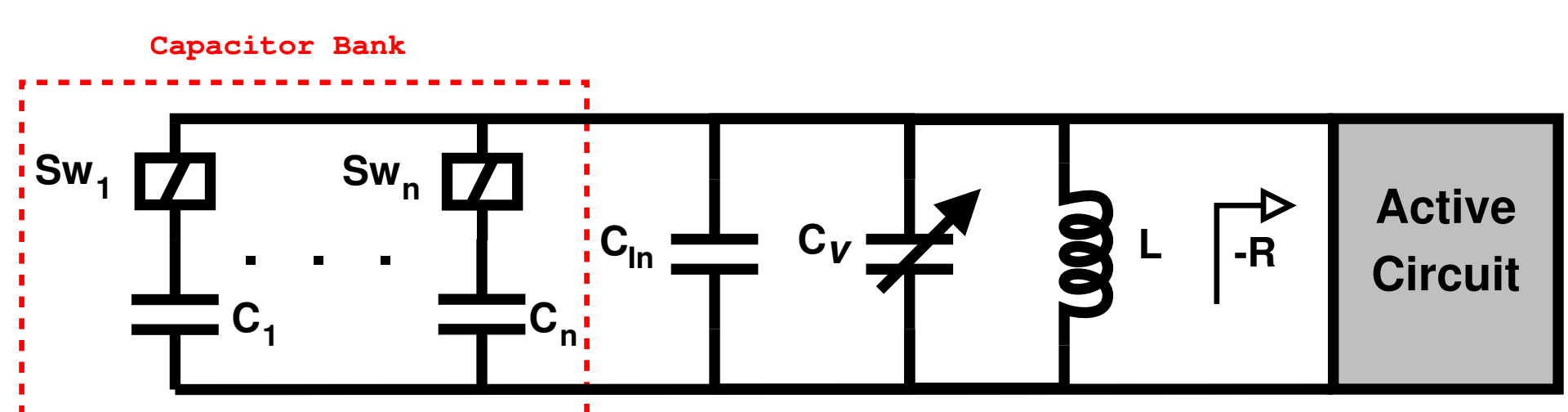
Section 2

The Figure below shows the parallel equivalent VCO resonant circuit, representing a parallel connection of a circuit inductance L, a varactor capacitance and capacitor(s) bank (C_v) and equivalent input transistor capacitance (C_{in}) (cross-coupled pMOS). Its impedance is expressed as:

$$Z_T(j\omega) = \frac{1}{\frac{1}{R_s} + j(\omega(C_v + C_{in}) - \frac{1}{\omega L})} \quad (1)$$



The negative resistance is synthesized from an active circuit, as illustrated in figure below.



Conclusion

The downscaling in CMOS technology has established challenging design conditions for each technology node, due to the rising demand for higher levels of operating performance with power reduction in telecommunication systems, and considering the trend for implementation of radio-frequency, mixed-signal and digital modules in fully integrated monolithic structures.

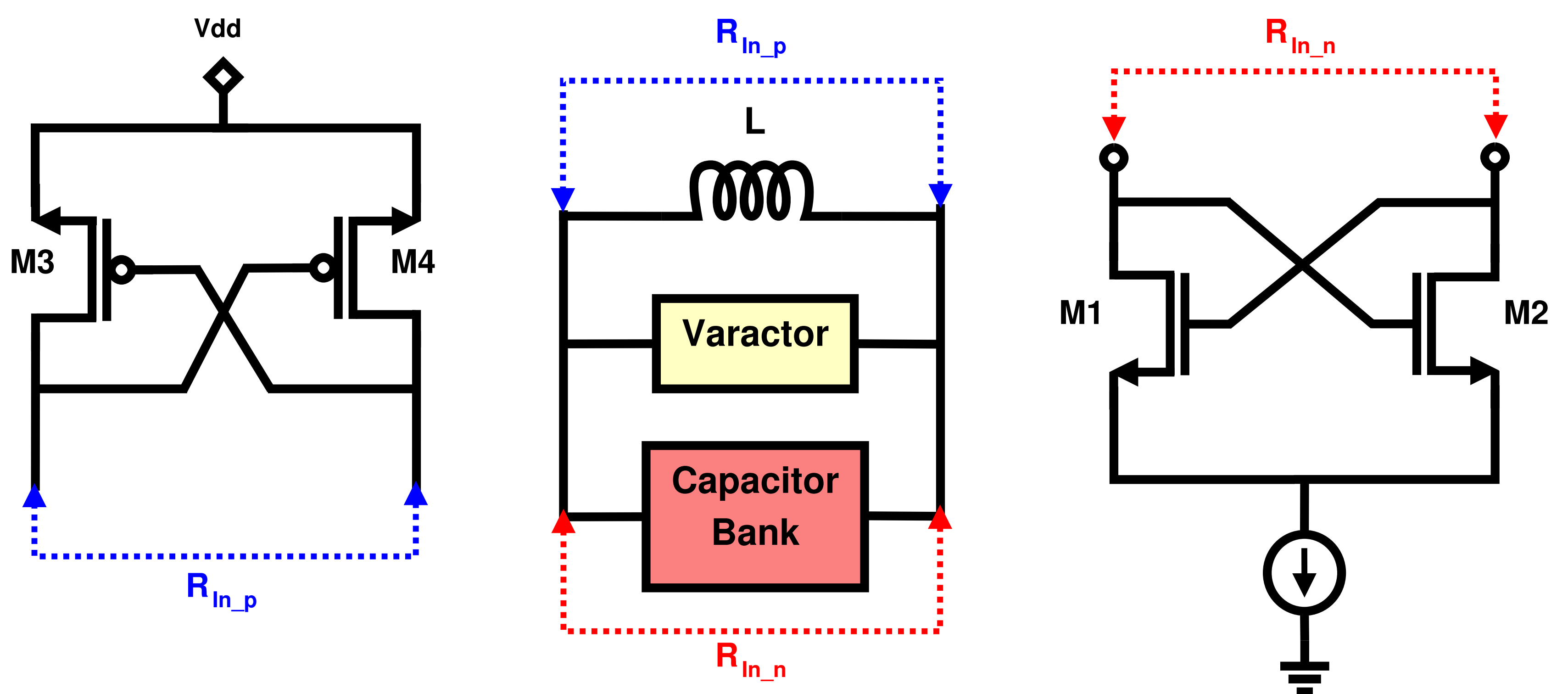
In this context, this work presented a set of design concepts for LC Resonance Voltage-Controlled Oscillators (LC-VCO) with self-biased output buffers for application in PLL-based Frequency Synthesizers. The obtained set of simulation environment-based results demonstrates the generation of output waveforms with high level of harmonic purity, and a frequency tuning characteristic with a proper linearity for a frequency range around 300 MHz.

Acknowledgment

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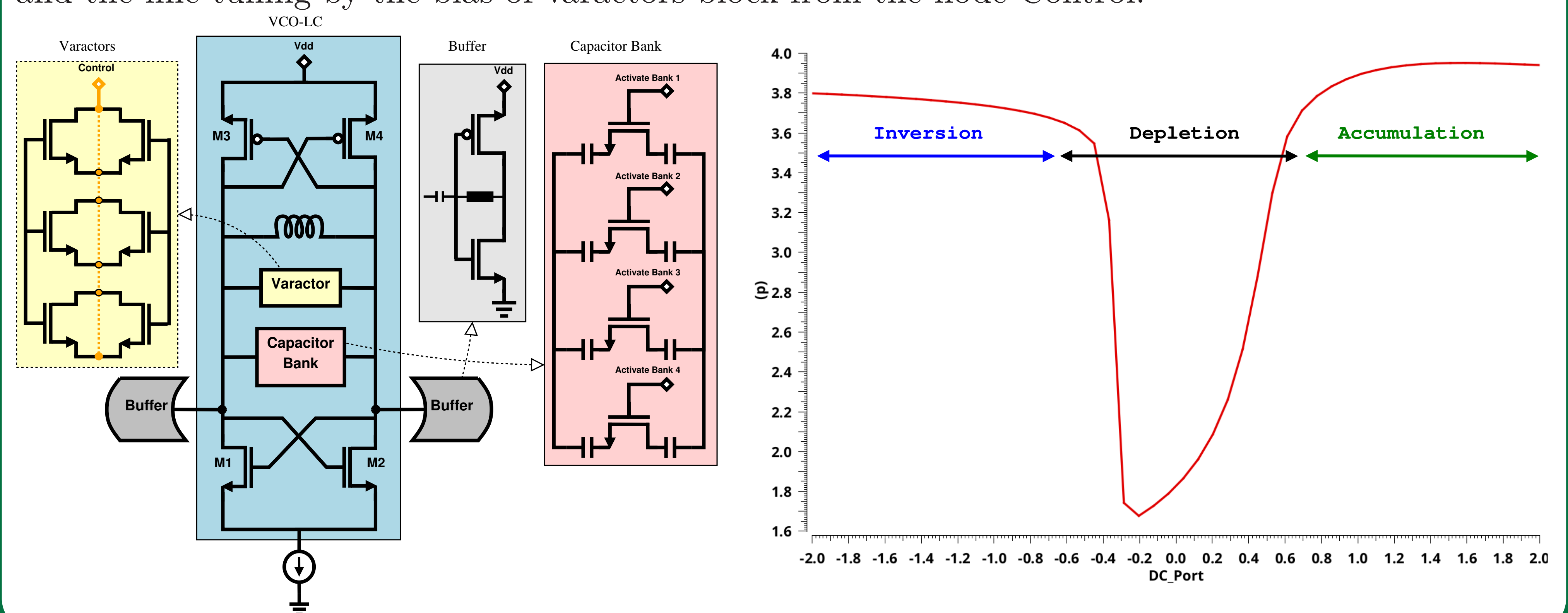
Methods

Both nMOS and pMOS pairs generate negative resistance to the LC-tank, R_{In_n} and R_{In_p} , respectively. The cross-coupled pairs are used in order to avoid the resistive losses that would cause the end of the oscillations. Which according to their polarization, allowed the flow of energy from the source to the tank circuit, thus renewing the energy dissipated constantly. Thus, the transistors supply positive feedback to the circuit. This feedback is modeled as a negative resistance, as seen in Figure below, Figure in section Implementation and Equation below. The use passive devices in addition to the nMOS or pMOS pair increases the noise sources and the parasitics so much that phase noise performance and frequency tuning characteristics are affected. Thus, to minimize these limits, only one active element was used in this project.



Materials

The proposed VCO consists of the following elements: high-quality inductor (L), digitally-switched capacitors block, varactors block that are made of nMOS transistors and cross-coupled transistors (pMOS and nMOS). The cross-coupled pair CMOS generates the negative impedance to cancel the energy loss in the LC tank. The inductor of the LC tank is realized using a inductor of 1.00 nH. Frequency tuning is achieved by two steps: coarse-tuning through a digitally-switched capacitor block and the fine-tuning by the bias of varactors block from the node Control.



Results

